CLAIMS

I claim:

1. A chip apparatus for use in a package comprising an ionic solution, the chip comprising

an insulating diaphragm,

one of a microscale and a nanoscale device disposed one of in or on the insulating diaphragm, and

a semiconductor frame supporting the insulating diaphragm,

wherein those portions of the semiconductor frame which are to be capacitively coupled to an ionic solution, the ionic solution also to be electrically coupled to the one of a microscale and a nanoscale device, comprise an n-type semiconductor.

2. A chip apparatus as claimed in Claim 1 wherein the n-type semiconductor comprises silicon.

3. A chip apparatus as claimed in Claim 2 wherein the silicon is doped with a dopant chosen from a group comprising phosphorous and arsenic.

4. A chip apparatus as claimed in Claim 1 wherein the n-type semiconductor is chosen from a group comprising germanium and gallium arsenide.

5. A chip apparatus as claimed in Claim 4 wherein the n-type semiconductor is doped with a dopant chosen from a group comprising phosphorous and arsenic.

6. A chip apparatus as claimed in Claim 1 wherein the one of a microscale and a nanoscale device comprises a nanopore.

7. A method of fabricating a chip for use in a package comprising an ionic solution, the method comprising

providing a semiconductor frame,

providing n-type semiconductor regions comprising those portions of the semiconductor frame which are to be capacitively coupled to an ionic solution,

providing an insulating diaphragm supported by the semiconductor frame, and

providing one of a microscale and a nanoscale device disposed one of in or on the insulating diaphragm, the ionic solution also to be electrically coupled to the one of a microscale and a nanoscale device.

8. A method as claimed in Claim 7 wherein the n-type semiconductor comprises silicon.
9. A method as claimed in Claim 8 wherein the silicon is doped with a dopant chosen from a group comprising phosphorous and arsenic.
10. A method as claimed in Claim 7 wherein the n-type semiconductor is chosen from a group comprising germanium and gallium arsenide.
11. A method as claimed in Claim 7 wherein the n-type semiconductor is doped with a dopant chosen from a group comprising phosphorous and arsenic.